Infrastructure IP for Configuration and Test of Boards and Systems

C.J. Clark and Mike Ricchetti
Intellitech Corp.

Editor's note:
Embedding infrastructure IP to optimize chip-level manufacturing test and debugging has recently become common practice. However, adopting the same approach for boards and systems requires a different family of infrastructure IP. This article introduces such a family and discusses how it can optimize manufacturing test and debugging, as well as support configurability, especially in today's reconfigurable products.
—Yervant Zorian, Virage Logic

ADVANCES in semiconductor technology and design automation, together with increased market competition, have driven engineers to achieve higher levels of integration with shortened development cycles. Expectations are that new products will have improved performance, more advanced features, and lower cost, when compared to the generation of products they replace. As a result, systems are becoming increasingly more complex, and corporations are striving for higher levels of productivity from engineering teams. This creates challenges for engineers to design electronic systems with higher performance and increased functionality, while reducing manufacturing costs and improving time to market. Structured embedded configuration and test for PCBs and systems offers the best methodology to achieve these high product expectations, if a parallel is drawn to the history of IC design and test. However, the opportunity costs and reduced engineering staff are making it increasingly difficult for engineers to dedicate time and resources to design and validate a robust system configuration-and-test solution on their own. Preengineered IP infrastructure for embedded configuration and test of complex PCBs and multiboard systems can help engineers meet these growing challenges.

On-chip infrastructure IP is increasingly becoming a viable solution for many IC design issues.[1] Yield and test concerns for very deep-submicron semiconductor technologies have forced chip designers to incorporate infrastructure IP into their designs to help with silicon debug, improve test quality, and increase manufacturing yield. Examples of such infrastructure IP include BIST for logic and memories, built-in self-repair (BISR) for embedded memories, embedded-core test logic for SoCs, and embedded timing analysis circuitry. IP infrastructure—dedicated infrastructure separate from the IC's functional circuitry—enables reuse in different designs. This reuse minimizes the time IC designers spend manually designing strategies for scan-based test. Design automation has facilitated the use of IP infrastructure, significantly reducing the IC DFT effort.

As PCBs and systems increasingly mimic more of an IC's characteristics—for example, having only peripheral physical access—board and system designers must confront many of the same issues IC designers face at the chip level. For example, advanced device packaging such as ball grid arrays (BGAs), along with the demand for product miniaturization, has made physical access to PCB and system nets extremely difficult, or even impossible. Traditional methods (physically probing interconnects) for prototype debugging and manufacturing test are no longer feasible.

Moreover, the higher clock speeds and data rates that come with increased performance and high-speed serial interconnects often prevent physical probing, because of signal integrity issues associated with the probes themselves. Performing only functional tests of these products yields the same results that IC designers discovered in the early 1990s: low fault coverage and long test development times.[2]

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These problems make infrastructure IP to support cost-efficient debug, configuration, and board and system test desirable. Although standards like IEEE 1149.1 (Standard Test Access Port and Boundary-Scan Architecture) and IEEE 1532 (Standard for In System Configuration of Programmable Devices) describe device-level operations for test and configuration, these standards do not specify a standard approach for accessing these devices on complex boards or in multiboard systems. Previous attempts to design infrastructure in-house have used ad-hoc methods and do not fully address the latest issues facing today's design engineers. Commercial ATE and PC-based boundary scan test equipment cannot easily accommodate the ad-hoc approaches, further increasing engineering time for configuration-and-test development, validation, and debug.

What is required is off-the-shelf, plug-and-play IP that allows scalable in-system configuration, debug, and test infrastructure that is openly understood by external ATE. System designers could then build in-the-field reconfigurable, high-quality, self-testable products, with minimal engineering time and effort. Furthermore, a unified test and configuration approach would enable field-adaptable products, lower the cost for manufacturing test and field support, and extend product lifetimes. Infrastructure IP for the board and system level could also reduce design risk, because the PCB and system configuration and test details are preengineered. The solutions could be scalable, and reusable in different designs, during all phases of the product life cycle.

Toward this end, we have created a complete development environment for structured, embedded configuration and test. This environment provides comprehensive infrastructure IP to create, validate, and apply system configuration-and-test suites based on IEEE 1149.1. Our methodology can be used throughout the entire product life cycle, to help design engineers bring up and debug prototype designs in the lab, to help manufacturers test products during volume production, to reconfigure products in the field, and to test and diagnose systems.

Problem overview

Methods and strategies for configuration and test play important roles in determining whether a particular solution is cost-effective. Many current approaches to configuration and test are struggling to keep up with the increasing complexity and cost constraints of today's boards and systems. A detailed discussion of the challenges using traditional approaches such as functional software-based test and in-house FPGA configuration methods is beyond this article's scope, but we provide such details in an earlier work.[3]

A traditional approach to embedded test is to store functional diagnostic code on-board the product (for example, in the CPU's Flash memory). Engineers use these embedded tests, in manufacturing and in the field, to test the integrated systems. These functional test programs are ad hoc, custom, embedded-software applications. Specialized resources are necessary to develop, validate, and maintain them, leading to high costs due to long development times and related engineering resources. Quality-assurance managers cannot deterministically measure the fault coverage of functional tests, and the risks of software-based functional tests are high. Although managers can invest significant resources, any software-based functional test that can't identify faults in the field or isolate faults enough to repair a failing PCB offers little value over running the system in mission mode and identifying that it doesn't function. Executing functional tests also requires a (mostly) working system; they offer limited value in system bring-up and debug. Thus, as system complexity increases, functional test for boards and systems alone is increasingly more impractical, just as testing digital ICs purely with functional test became impractical.

Structured, embedded configuration and test

Our approach provides a structured methodology for embedding configuration and test at the board and system levels, which creates cost efficiencies over the entire product life cycle. This saves time in design, test engineering development, and test execution. By including dedicated infrastructure IP in products, board and system designers can simplify in-system device configuration while enabling comprehensive structural test throughout the system. Our approach provides a scalable, reusable methodology that augments existing test and configuration standards. The embedded configuration-and-test architecture offloads in-circuit test (ICT) equipment so that structural digital test and device configuration can occur in-system (which is more cost-effective), and expensive ICT equipment can be better leveraged for analog testing. Our infrastructure IP provides a needed foundation for embedded structural tests that minimizes functional test development. In developing our architecture, our goal was to build an IP infrastructure that would

- be completely scalable and reusable at any level of integration;

- support anytime/anywhere testing, and in-the-field reconfiguration for an entire multiboard system;
- enable scalable, highly parallel test and configuration to reduce reconfiguration times in the field and eliminate throughput bottlenecks in production test;
- provide a foundation of high-fault-coverage structural test on which to build functional test and diagnostics firmware;
- support in-system, at-speed interconnect testing without the signal integrity problems associated with ICT fixtures;
- automatically create and validate embedded tests and configurations, reducing cost and allowing reuse any time during a product's life cycle; and
- considerably reduce or eliminate the need for physical access.

To implement our methodology, we provide a family of patent-pending infrastructure IP, which engineers can embed as cores or use as ICs for the board and system levels of their products. The basic building blocks include a scan-ring linking device, an embedded configuration-and-test processor, a fast access controller, and a parallel-test bus controller.

Board-level scan-ring partitioning

Commercial devices for linking IEEE-1149.1-compliant scan chains have existed since the early 1990s.[4-5] Devices such as National Semiconductor's Scan Bridge or Texas Instruments' Scan Path Linker connect three or four scan chains into a single path for PCB-level interconnect testing. They can link the scan chains, or permit the enabling of the secondary scan chains (also called scan rings) one at a time to reduce scan chain lengths for in-system configurations. However, the small number of scan rings, fixed 3.3-V voltage levels, and an inadequate distribution of critical signals for high-speed IEEE 1149.1 operations limit the use of these devices in today's designs.

Our scan-ring linking device gives PCB designers infrastructure IP to easily partition scan paths at the board level. The architecture goals of this infrastructure IP include

- the ability to embed it into a complex programmable logic device (CPLD), FPGA, or ASIC, and configure it to accommodate multiple voltage levels on *N* scan chains—thus reducing parts costs, saving board area, and providing a flexible implementation;
- better signal integrity and performance through its distributed handling of global test access port (TAP) signals TCK (test clock), TMS (test mode select), and TRST (test reset);
- a single entry point for IEEE 1149.1 access, allowing boundary scan access without the need for expensive or lower performance, ICT fixtures, or equipment;
- a scan ring linker that is fully testable and configurable with the associated external IEEE 1149.1 test development tools;
- an interface to CPU scan chains so that emulation equipment can work hand-in-hand with IEEE-1149.1-based hardware debuggers;
- direct access to all IP I/Os to allow easy in-system testing of the IP; and
- full compatibility with other infrastructure IP components.

The linking device IP connects any number of scan rings into a single path. A single IEEE 1149.1 external interface then allows independent testing and configuration of devices on secondary scan chains. This dramatically shortens scan operation time and maximizes data throughput. The linking device also provides the proper buffering of test signals, eliminating the need for additional external components on the board. These additional external components—commonly required by commercial devices like Scan Path Linker and Scan Bridge—create untestable pins, such as those for buffers and voltage-level translators.

At the PCB level, the linking device can reduce the complexities and costs of designing IEEE 1149.1 test infrastructure for products requiring multiple scan chains. Designers can configure this IP to handle the required number of scan paths, voltages, and so on. It is fully compliant with the IEEE 1149.1 standard, and it provides a plug-and-play solution for PCB designers who use multiple scan chains.

Figure 1 shows an example scan chain configuration at the board level using the linking device. The figure illustrates how the linking IP can handle multiple scan chain partitions with different voltage requirements. Placing FPGAs, CPLDs, and ASICs on separate chains helps reduce the configuration times. It also facilitates keeping ill-behaved devices on other chains in their safe states while programming other devices. Additionally, some vendor devices are not programmable when devices from other vendors are in the same chain, so the former must be on separate board-level scan chains. Designers can also place processors on a separate

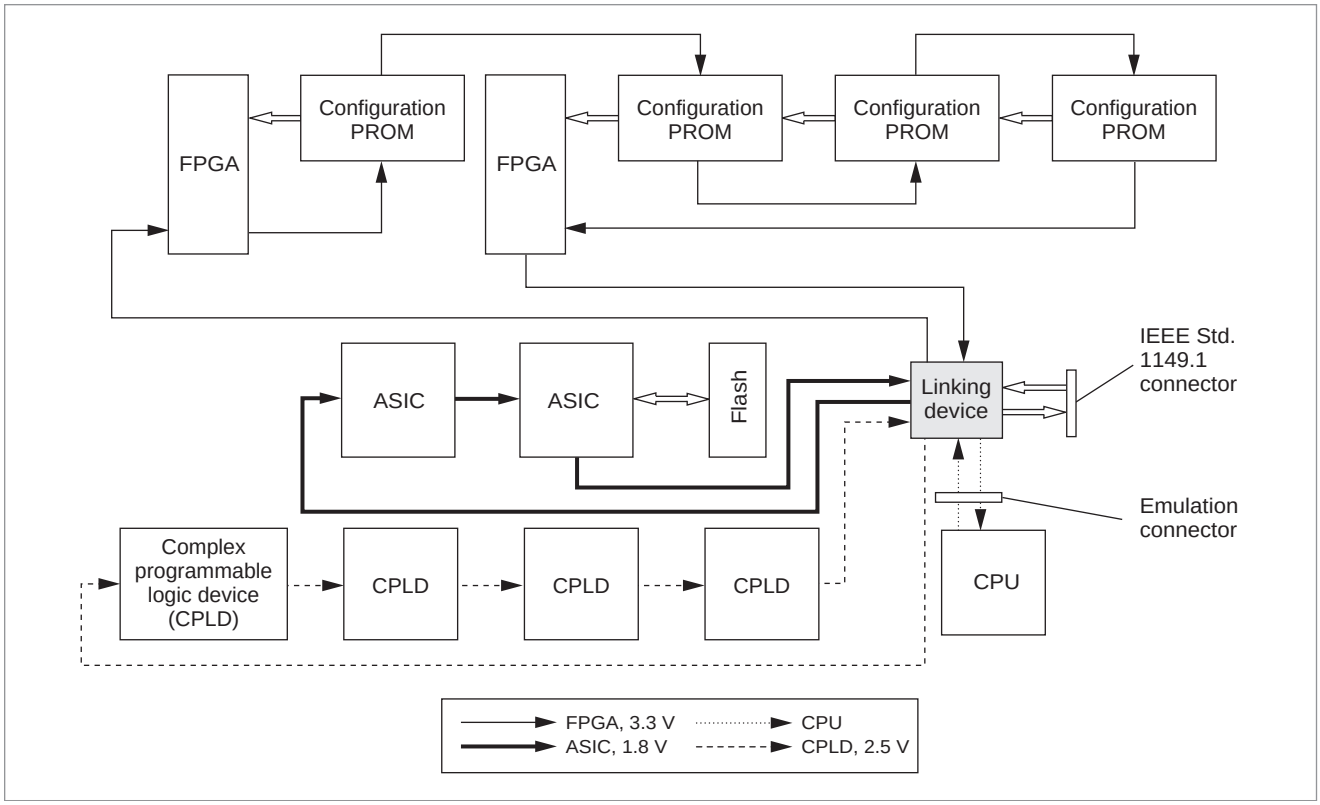

Figure 1. Scan chain configuration for a single board.

chain, allowing control of the CPU for emulation (through a dedicated, stand-alone emulation connector). The linking device provides access to the rest of the chains and on-board logic for hardware debugging while using the CPU emulation connector.

Centralized and embedded configuration-and-test management

Researchers have estimated that a PCB is tested up to seven times during its product life.[6] This information, coupled with the desire to perform these tests in geographically dispersed areas, provides a compelling reason to embed testing into the PCB itself. Our dedicated and embedded configuration-and-test processor centrally manages configuration and testing of PCBs and systems.[7] There are many dedicated special-purpose processors in systems today—for example, network processors, audio processors, DSPs, and video processors. There are many advantages to using such processors over simply using a mission mode, general-purpose CPU for these tasks. Dedicated architectures for embedded test enable testing general-purpose CPUs, testing the related CPU logic, and logging all failures—all without requiring a functioning system. Our configuration-and-test processor is designed around a novel architecture and is interoperable with all other IP infrastructure blocks. It lets engineers develop and validate manufacturing tests and device configuration suites with automated PC-based tools and then automatically embed them into the system.

Our goals in designing this embedded processor were as follows:

- Develop a cost-effective, codeless processor that reduces engineering design effort.
- Provide a scalable, reusable methodology that supports centralized anytime/anywhere reconfiguration and test of an entire system.
- Reduce board area and cost of parts for FPGA and CPLD configurations.
- Leverage IEEE 1149.1 and IEEE 1532 to provide vendor-independent device configurations.
- Manage different preprogrammed system designs so that designers can create in-field configurable products.
- Provide detailed diagnostic data to enable PCB and system repair.
- Enable integration with other infrastructure IP blocks.

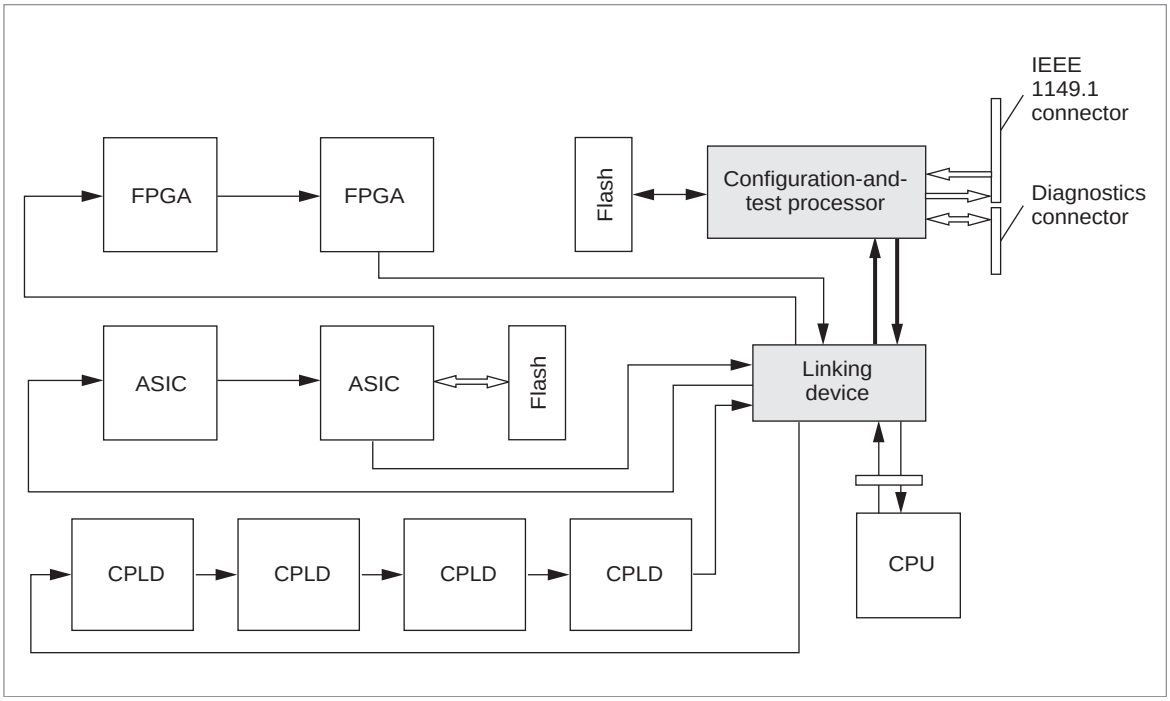

Figure 2. Embedded configuration-and-test processor for a single PCB system.

In production manufacturing, board-level device configuration and testing would typically be run on ICT. However, embedding a dedicated configuration-and-test processor can eliminate the need to run configuration and digital tests on ICT equipment. This lowers manufacturing costs by greatly reducing the time a board spends sitting on expensive capital equipment. Embedded test also allows the same high-quality tests to handle many different environments and all phases of the product's life cycle. These include lab prototyping, volume PCB manufacturing, system integration, vibration test, highly accelerated life test (HALT) and highly accelerated stress screen (HASS) test, power-up self-test, field service, and depot repair. Our embedded processor can also manage multiple system configurations, making system reconfiguration possible anywhere, and engineering changes can easily be made at any time during a product's life cycle.

We designed the configuration-and-test processor to be a vendor-independent solution, leveraging the new IEEE 1532 standard and eliminating the need for proprietary programmable ROM (PROM) or Flash-memory-based solutions. With this infrastructure IP, designers no longer need to develop customized solutions for embedded in-system configuration, thereby reducing development time. A single configuration-and-test processor at power-up or under CPU control can automatically run the entire manufacturing test stream, including scan tests, logic and memory BIST, and board or system interconnect tests. In addition, the processor can configure all the programmable logic in the system, effectively building configuration and test into the product.

Figure 2 shows an example of how this processor works at the board level. The dedicated processor replaces the configuration PROMs, and interfaces with a Flash-memory device. This device stores test and configuration suites and drives the IEEE 1149.1 bus to the linking device, which links the multiple scan chains on the board. The processor also interfaces with an external IEEE 1149.1 connector, which allows communication to and from external development and validation tools. This IEEE 1149.1 interface is used to develop and validate configuration-and-test vectors with traditional external PC-based toolsets. This is a major advantage in that the external boundary scan tools can communicate through the processor directly to the linking device. Therefore, this guarantees the equivalent drive and signal integrity for the on-board configuration-and-test mechanism (that is, the configuration-and-test processor, and Flash), as was achieved with the external PC-based tools. The result is that just one configuration-and-test validation step is necessary, eliminating the need for revalidating tests and configuration in the embedded environment.

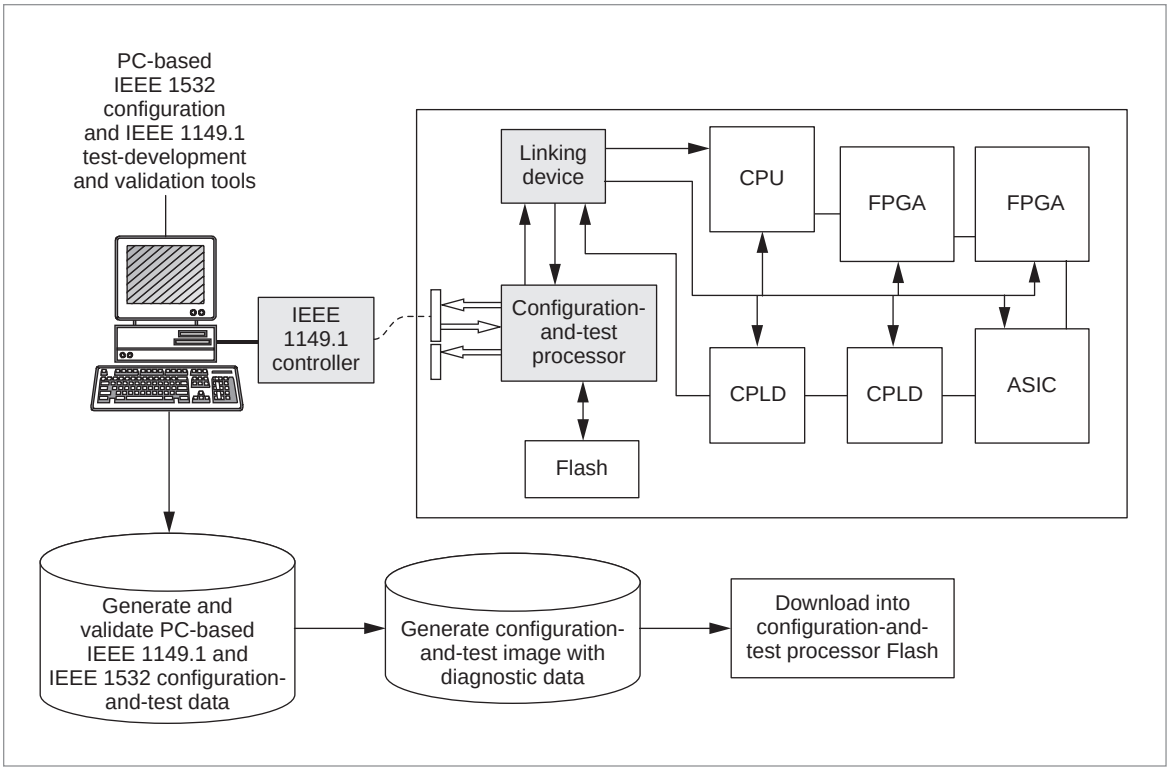

Figure 3. Optimized embedded configuration-and-test flow.

After engineers finalize the test and configuration suites, they are downloaded into the Flash memory for embedded execution. Subsequently, the external IEEE 1149.1 equipment is unplugged, and the processor has control of running the embedded test suites and programming the FPGAs. This architecture provides flexible completion and failure indications, including go/no-go LEDs, 7-segment LED displays for diagnostic failure codes, and a serial port for text-based diagnostics. The diagnostics information, suitable for field-replaceable unit (FRU) replacement or PCB repair, is embedded along with the configuration-and-test data. This approach to embedding test and configuration uses a codeless architecture, thereby reducing engineering time. The same test and configuration vectors developed with the external tools are reused by embedding them in Flash memory.

Figure 3 shows how the configuration-and-test processor connects to external, automated development tools for developing and validating configuration data and test programs. The figure also shows our architecture's use model and flow, which is much simpler than the test flow required in using test bus controllers, such as National Semiconductor's PSC100 or Texas Instruments' ACT8980,[8] that interface to general-purpose microprocessors. We use traditional PC-based IEEE 1149.1 software tools for ATPG and debug. This development environment then interfaces with an IEEE 1149.1 external controller, which connects to the PCB.

In Figure 3, the PCB has implemented the configuration-and-test processor as a separate device from the linking device. However, when desirable, designers can combine the scan-ring linking IP with the processor IP to create a single packaged-chip solution.

Fast Flash-memory programming

We designed a complementary infrastructure IP module, the fast access controller (FAC), to enable high-speed, high-throughput in-system configuration and test of external Flash and other memories.[9] The FAC allows fast on-board programming by using advanced data deserialization and a programmable control protocol to minimize the number of scan operations and the amount of serial scan data required during Flash-memory programming and memory testing. The FAC can then program Flash-memory devices in the system over an IEEE 1149.1 bus at speeds equivalent to those achieved by off-board and direct-access programming techniques. Its memory protocols are fully configurable in the system, through PC-based boundary scan tools.

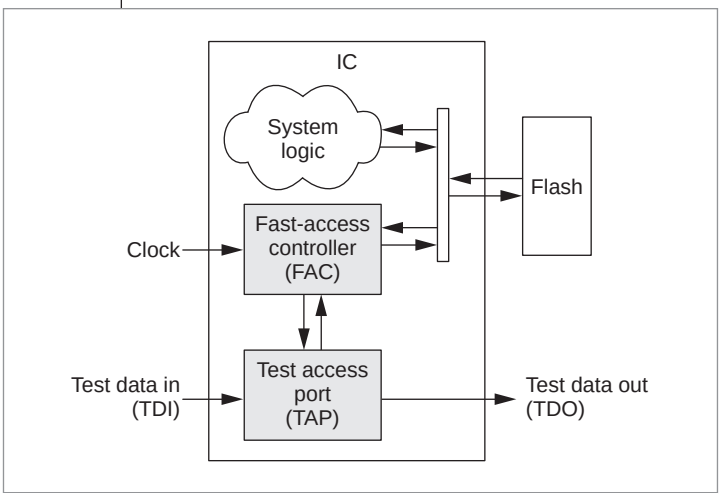

Figure 4. Fast access controller (FAC) module.

The FAC is also customizable, depending on the application, so it can support access to a wide variety of Flash and other memory devices. With its programmability, a single FAC can even access multiple memories.

Figure 4 shows a block diagram of the FAC embedded in an IC. The FAC interfaces with the chip's IEEE 1149.1 TAP controller and, in this example, an external Flash memory. The interface to Flash memory is through a multiplexer that selects between the system logic and the FAC. The FAC leverages the serial IEEE 1149.1 test infrastructure to access the memory in parallel. The FAC method is scalable and can achieve optimal programming throughput of Flash-memory devices, even with low (less than 3 MHz) test clock rates. In addition, the scan length or number of IEEE 1149.1 devices in the PCB's boundary scan chain does not affect the FAC architecture. The FAC enables the IEEE 1149.1 bus to act as a central, high-speed serial bus for in-system configuration of all on-board Flash-memory devices. Furthermore, it eliminates the performance issues associated with IEEE-1149.1-based in-system Flash-memory programming in an Extest approach.

The FAC provides a plug-and-play IP solution for processor, ASIC, SoC, and FPGA designers. FPGA designers can temporarily download the FAC, allowing fast programming access to a Flash-memory device, and afterward, reprogram the normal system design back into the FPGA. The method is compatible with our other infrastructure IP. For example, the embedded configuration-and-test processor can use the FAC to give designers a complete embedded solution for in-system Flash-memory programming and configuration of CPLD and FPGA devices.

The use of memory devices in today's electronic products, including embedded SRAM or DRAM memories and nonvolatile memories such as Flash, is growing. Consequently, for debug and in-production manufacturing, fast test access to large memories and Flash programming is becoming essential. Compared to the FAC, traditional methods are more costly, and programming times are longer. In addition, the FAC allows reuse during all phases of a product's life cycle, whereas other methods do not. With the FAC, designers and test engineers can reprogram Flash-memory devices during prototype bring-up, in production manufacturing, or in the field, all with a unified methodology.

Parallel configuration and test

Our infrastructure IP incorporates novel capabilities to improve configuration and test of multiboard systems and greatly improve throughput in production manufacturing. Here, we describe these capabilities and how they improve upon current methods.

Multiboard systems

For multiboard systems with backplanes and removable PCBs, configuration-and-test access is important, not just for each individual board, but also for the entire system. This includes testing board-to-board interconnects and optimizing configuration and test at the system level.

Although each board in a multiboard system has partitioned scan chains and a board-level access port (through the scan-ring linking device), accessing these board-level scan chains at the system level requires a way to chain the boards together. Here, we must consider the system's configuration, because it could have optional boards in the backplane. The problem is that when a board is absent, it leaves an open slot in the backplane, breaking the scan chain if the boards are simply in series. The solution is to use a multidrop IEEE 1149.1 bus.

Figure 5 shows the signal connections for this style of bus. In addition to each of the global TAP signals (TCK, TMS, and TRST) getting connected as bused signals, the test data in (TDI) and test data out (TDO) are also connected as bused signals. Consequently, an open slot in the backplane will not break the TDI or TDO connections to other system boards. Because TDI and TDO are bused signals, each of the *N* PCBs in Figure 5 receives the exact same test data input stream on TDI, and only one PCB can drive TDO back onto the bus at a given time. Other PCBs that do not drive must keep their TDO inactive on the bus. Hence, some device in the system

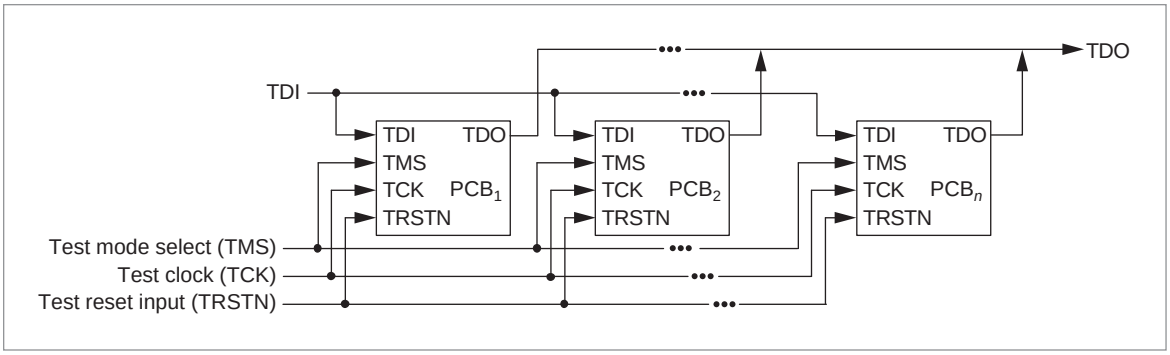

Figure 5. Multidrop scan bus for multiboard system.

must enable the addressing or selection of particular boards to receive configuration-and-test data and to send TDO responses. Typically, special addressable devices, such as Texas Instruments' ACT8996 or National Semiconductor's Scan Bridge PSC110F, handle this function.[10] We define the detailed aspects of our particular multidrop architecture in our patent application.[11]

Parallel-test bus controller

To address configuration and test for multiple board systems, we developed the parallel-test architecture (PTA)[11] to

- support parallel test and configuration of PCBs over the IEEE 1149.1 multidrop bus;
- provide system-level, multivendor PCB identification and addressing over this bus;
- support reusable PCB-to-PCB interconnect tests in dynamic systems;
- simplify signal integrity issues on multidrop backplanes;
- provide direct access to all IP I/Os to allow easy in-system testing of the IP itself; and
- enable integration and use with other infrastructure IP blocks.

The PTA infrastructure IP's main component is the parallel-test bus controller (PTBC). The most innovative feature of the PTA is that it allows parallel configuration and testing of the same type of PCBs over a standard IEEE 1149.1 multidrop bus—for example, you could simultaneously configure and test 10 like PCBs within a system. The obvious benefit of this is that it reduces configuration-and-test times dramatically, lowering the overall cost of the product. If it takes 2 minutes to configure and test a single PCB, it takes only 2 minutes to configure and test 10 PCBs in a chassis, not 20 minutes. This novel implementation of IEEE 1149.1 test can be realized in a few hundred additional flip-flops and gates in an ASIC or FPGA design. Unlimited parallel test over an IEEE 1149.1 interface has considerable utility in other areas of digital test, such as for high-volume consumer products and even ICs. A discussion of these other uses is, however, beyond the scope of this article.

The PTBC also supports position-independent, board-to-board interconnect testing with specialized instructions to optimize access between boards. In PCB-to-PCB interconnect testing with multidrop ICs from TI and National Semiconductor and others, system-level interconnect tests are not reusable, because the test patterns incorporate each PCB's physical address. For example, three PCB types (or three versions of the same type) designed for a four-slot system, where the PCBs can plug into the system in any combination, would require some 3^4, or 81, possible system-level interconnect tests. The PTBC-based system, on the other hand, requires only six interconnect tests for any system built or updated in the field.

Another important aspect not addressed by commercial multidrop devices is integrated PCB identification over IEEE 1149.1. In multivendor systems, such as those based on cPCI (Compact Peripheral Component Interface) or VME (VersaModule Eurocard), vendors must provide unique identification for their PCB over the multidrop bus. Designers have developed ad hoc methods of PCB identification and PCB addressing through I^2C (Inter-Integrated Circuit) buses, serial PROM, and other functional methods. When embedded test mechanisms cannot easily access and control these approaches, or when they're not compatible with standard test development tools, the complexity of configuration-and-test development increases dramatically. Architectures that require bringing up the system to perform this identification end up slowing down manu-

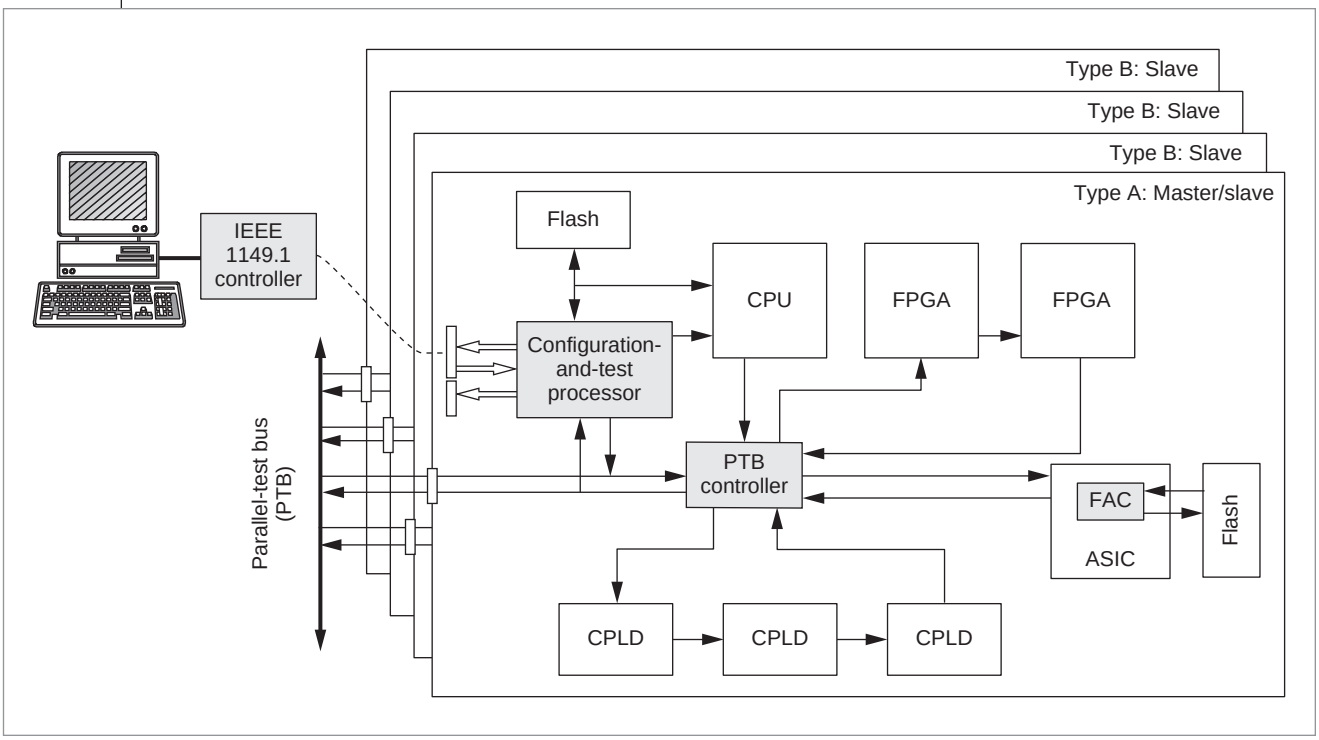

Figure 6. Optimized architecture for embedded configuration and test of a multiboard system.

facturing throughput; they are of little use in the field when systems fail to boot or for the logging of failures.

The PTA and PTBC support vendor-independent PCB identification. Multivendor PCB identification is critical for embedded configuration-and-test processors to automatically identify what PCBs are present in a dynamic system and decide which tests and configuration data to apply. The PTBC IC is packaged to be implemented on PCBs that are designed as plug-in blades in a backplane-based system.

Figure 6 shows a multiboard system based on the PTBC. The PTBC interfaces to the bused IEEE 1149.1 signals through the system backplane. The slot-addressing inputs and type identification inputs are not shown in the figure. The PTBC also links the scan chain partitions on the PCB by integrating the board-level scan-ring linking device with the PTBC IP. Each system board has an onboard PTBC and a multidrop connection to the parallel-test bus. Engineers can use the external IEEE 1149.1 controller and embedded processor for validation before embedding the configuration-and-test data. In this architecture, the configuration-and-test processor enables embedded system-level parallel configuration, standalone PCB self-test on all master/slave PCBs (type A in the figure), embedded parallel test, and system-level interconnect test. When slave PCBs have a local configuration-and-test processor, it's possible to test, in parallel, similar and dissimilar PCBs in a system. Systems are also permitted to have multiple master/slave PCBs, in which case the master may be determined on the fly. The system in Figure 6 provides optimal test and configuration times with minimal FPGA configuration validation, easy access for prototype debugging, straightforward interconnect test development with a minimum number of tests, and configuration and test of the entire system separate from mission mode logic (enabling in-field fault logging). Centralized control over logic and Flash-memory configuration enables in-field upgrades and simple pre-embedding validation that uses external IEEE-1149.1-based tools.

THE INFRASTRUCTURE IP presented here is interoperable, in that each member of the family was built to work with the others and independent of system operation. Any of them can be used alone, or combined into an integrated solution. The IP will lower the overall product costs, reduce configuration-and-test time, and provide new methodologies that improve current approaches. Key to the infrastructure IP is its reuse, both in terms of the IP itself and the reuse of configuration-and-test suites in all phases of the product life cycle, from prototype bring-up to the field. ■

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C.J. Clark is president and CEO of Intellitech Corp. His professional interests include DFT, BIST, and FPGA configuration. Clark has a BS in electrical and computer Engineering from the University of New Hampshire. He is a member of the IEEE 1149.4, IEEE 1532, and P1500 working groups, and a past chair of the IEEE 1149.1 working group. He also serves on the University of New Hampshire College of Engineering and Physical Science (CEPS) Advisory Board and the UNH Department of Electrical Engineering Advisory Board.

Mike Ricchetti is CTO at Intellitech Corp. His research interests include DFT architecture, core test, BIST, and DFT-focused testers. Ricchetti has a BS in electrical engineering from Ohio State University. He is a member of the IEEE P1500 and IEEE 1149.6 working groups, and he chairs the IEEE Test Technology Technical Council Technical Activities Committee on Silicon Debug and Diagnosis.

■ Direct questions and comments about this article to C.J. Clark, Intellitech Corp., 70 Main St., Durham, NH 03824; cjclark@intellitech.com.